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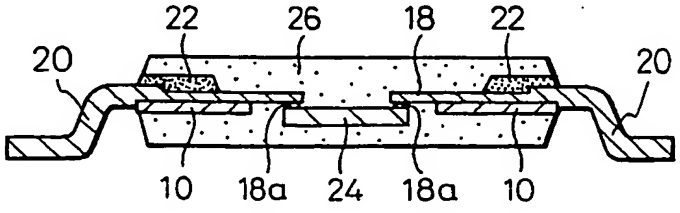

(57) Abstract

In a lead frame adapted to be used for a semiconductor device, a plurality of inner leads (18) are made of a thin conductive material for easily forming a fine pattern of the inner leads. A plurality of outer leads (20) are integrally formed with the respective inner leads. The outer leads are coated with metal layers to increase the thickness thereof, so that a desired strength of the outer leads is obtained. A semiconductor chip (24) is electrically connected to the inner leads. The semiconductor chip and a part of the lead frame including the inner leads are hermetically sealed with a resin (26) and, thus, a semiconductor device is obtained.

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DESCRIPTION

Lead Frame and Semiconductor Device Using Same

TECHNICAL FIELD

The present invention relates to a lead frame and a semiconductor device using the same lead frame. This invention also relates to a process for making such a lead frame.

BACKGROUND ART

In the field of lead frames adapted to be used for a semiconductor device, since semiconductor chips have become highly integrated, multi-pin lead frames having a large number of leads and a fine lead pattern structure have been developed and produced. In this connection, in order to make a fine lead pattern structure on a lead frame, a relatively thin material has been used as a lead frame base and an etching process has been widely adopted to form such fine micro-patterns, since the etching process is more suitable than the other processes, such as a punching process, to easily form such fine patterns.

In a conventional method for manufacturing a lead frame, however, there has been a limitation on forming a very fine lead pattern. Thus, a TAB (tape automated bonding) tape lead frame has been developed and used, on which a finer pattern could be formed than on a conventional metal lead frame.

A TAB tape can be made by forming a thin conductive film on an electrically insulative base film and etching the conductive film to form a desired conductive pattern. Using such a TAB tape, since the conductive patterns are supported on a thin flexible base film, the thickness of such conductive patterns can be reduced to about several tens of μm. Thus, it becomes possible to make very fine patterns of leads which could not be attained on a conventional metal lead frame.

On the other hand, a semiconductor device is conventionally made as follows. After the inner leads of

the lead frame are electrically connected to the semiconductor chip by a wire-bonding process, the lead frame is hermetically sealed with resin to obtain a product. In a case where a TAB tape is used, the lead frame is also hermetically sealed with resin to obtain a semiconductor device product.

However, as mentioned above, since a TAB tape includes a plurality of leads which are made of conductive thin film, there has been a problem that a strength of leads are not sufficient and it is difficult to handle the same, such as when the product is mounted on a printed circuit board.

The above-mentioned problems concerning a TAB-tape also appear when a so-called single-layer-type TAB tape is used to make a lead frame, in which the leads are formed of a very thin conductive material with a thickness of not more than 100μm.

In addition, after the leads have been formed, it is necessary to prevent the leads from being deformed or bent. Thus, it becomes necessary that the outer leads have a certain strength to stably and accurately mount the product on a printed circuit board without any deformation of the leads.

DISCLOSURE OF INVENTION

An object of the present invention is to provide a lead frame and a semiconductor device using the same lead frame, in which the lead frame can be easily handled, as if it was a lead frame using a TAB tape or thin material, so that a semiconductor device product using such a lead frame can easily be mounted on a printed circuit board.

According to one aspect of the present invention, there is provided a lead frame adapted to be used for a semiconductor device comprising: a plurality of inner leads made of a thin conductive material for easily forming a fine pattern of said inner leads; and a plurality of outer leads integrally formed with said respective inner leads, said outer leads being coated

with metal layers to increase the thickness thereof, so that a desired strength of said outer leads is obtained.

According to another aspect of the present invention, there is provided a lead frame adapted to be used for a semiconductor device comprising: an insulating base film; a conductive pattern formed on said insulating base film, said conductive pattern including a plurality of inner leads and a plurality of outer leads integrally formed with said respective inner leads; and said inner leads being relatively thin, but said outer leads being coated with metal layers to increase the thickness thereof, so that a desired strength of said outer leads is obtained.

According to still another aspect of the present invention, there is provided a process for making a lead frame adapted to be used for a semiconductor device: comprising the following steps of: forming a conductive layer on an insulating base film; etching said conductive layer to form a conductive pattern including a plurality of inner leads and a plurality of outer leads integrally formed with said respective inner leads; and coating said outer leads with metal layers to increase the thickness of said outer leads, so that a desired strength of said outer leads is obtained.

According to further aspect of the present invention, there is provided a process for making a lead frame adapted to be used for a semiconductor device: comprising the following steps of: forming a conductive layer on an insulating base film having a device hole at a central position thereof and window holes located apart from said central device hole; etching said conductive layer to form a conductive pattern including a plurality of inner leads and a plurality of outer leads integrally formed with said respective inner leads, so that each said inner lead extends inward into said central device hole and each said outer lead extends outward from said inner lead over said window hole; and coating said outer

leads with metal layers to increase the thickness thereof, so that a desired strength of said outer leads is obtained.

According to still further aspect of the present invention, there is provided a process for making a lead frame adapted to be used for a semiconductor device: comprising the following steps of: forming a conductive layer on an insulating base film having window holes located apart from a central position of said base film; etching said conductive layer to form a conductive pattern including a die-pad located at a central position of said insulating base film, a plurality of inner leads and a plurality of outer leads integrally formed with said respective inner leads, so that each said inner lead extends toward said die-pad and each said outer lead extends outward from said inner lead over said window hole; and coating said outer leads with metal layers to increase the thickness thereof, so that a desired strength of said outer leads is obtained.

According to still another aspect of the present invention, there is provided a semiconductor device comprising: (a) a lead frame adapted to be used for a semiconductor device comprising: a plurality of inner leads made of a thin conductive material for easily forming a fine pattern of said inner leads; and a plurality of outer leads integrally formed with said respective inner leads, said outer leads being coated with metal layers to increase the thickness thereof, so that a desired strength of said outer leads is obtained; (b) a semiconductor chip electrically connected to said inner leads; and (c) a resin for hermetically sealing said semiconductor chip and a part of said lead frame including said inner leads.

According to still another aspect of the present invention, there is provided a semiconductor device comprising: (a) a lead frame comprising: an insulating base film having a device hole at a central position

thereof and window holes located apart from said device hole; a conductive pattern formed on said insulating base film, said conductive pattern including a plurality of inner leads and a plurality of outer leads integrally formed with said respective inner leads, so that each said inner lead extends inward into said central device hole and each said outer lead extends outward from said inner lead over said window hole; and said inner leads being relatively thin, but said outer leads being coated with metal layers to increase the thickness thereof, so that a desired strength of said outer leads is obtained; (b) a semiconductor chip mounted on and electrically connected to said inner leads within said central opening; and (c) a resin for hermetically sealing said semiconductor chip and a part of said lead frame including said inner leads.

According to still another aspect of the present invention, there is provided a semiconductor device comprising: (a) a lead frame comprising: an insulating base film having window holes located apart from a central position of said base film; a conductive pattern formed on said insulating base film, said conductive pattern including a plurality of inner leads and a plurality of outer leads integrally formed with said respective inner leads, so that each said inner lead extends toward said die-pad and each said outer lead extends outward from said inner lead over said window hole; and said inner leads being relatively thin, but said outer leads being coated with metal layers to increase the thickness thereof, so that a desired strength of said outer leads is obtained; (b) a semiconductor chip mounted on said die-pad; (c) bonding wires for electrically connecting said semiconductor chip to said inner leads; and (d) a resin for hermetically sealing said semiconductor chip and a part of said lead frame including said inner leads.

BRIEF DESCRIPTION OF DRAWINGS

Figures 1A-1D are plan views of some embodiments of a lead frame according to the present invention;

Figures 2A-2D are plan views of embodiments of a semiconductor device using a lead frame shown in Figs. 1A-1D, respectively, according to the present invention;

Figure 3 is a cross-sectional view of a semiconductor device shown in Fig. 2A or 2B;

Figure 4 is a cross-sectional view of a semiconductor device shown in Fig. 2C or 2D;

Figures 5A-5C are cross-sectional views of some variations of a lead frame according to the present invention;

Figures 6A-6D are cross-sectional views of some variations of an inner lead-bonding type semiconductor device according to the present invention;

Figure 7 is a cross-sectional view of an embodiment of a wire-bonding type semiconductor device according to the present invention;

Figure 8 is a cross-sectional view of another embodiment of a wire-bonding type semiconductor device according to the present invention;

Figures 9A-9D are cross-sectional views of some variations of a potted type semiconductor device;

Figure 10 is a cross-sectional view of another embodiment of a potted type semiconductor device;

Figure 11 is a cross-sectional view of an embodiment of an inner lead-bonding type semiconductor device having a heat spreader or heat sink;

Figure 12 is a cross-sectional view of an embodiment of a wire-bonding type semiconductor device having a heat spreader; and

Figure 13 is a cross-sectional view of another embodiment of a wire-bonding type semiconductor device having a heat spreader.

BEST MODE FOR CARRYING OUT THE INVENTION

Referring now to the drawings, wherein Figs. 1A-1D

are plan views of some embodiments of a lead frame constituted as a TAB tape according to the present invention. The TAB tape comprises an electrically insulating flexible base film 10, made of a material such as a polyimide, and an electrically conductive pattern formed on a surface of the base film. The conductive pattern having a desired pattern can be formed by any conventionally known method, such as by etching the conductive thin film attached on the base film 10. In order to attach a thin conductive film onto the base film, any known method can be used, such as a sputtering, vapor deposition, or adhering a copper foil onto the base film using any suitable adhesive.

The base film 10 of the (inner lead bonding type) TAB tapes shown in Figs. 1A and 1B is first provided with a device hole 12 at the central position of the TAB tape, four window holes 14 located apart from the device hole and symmetrically arranged to each other, and sprocket holes 16 equidistantly and regularly arranged at the edges of the TAB tape. A copper foil is then adhered to the base film 10 and etched to obtain a desired conductive pattern. The conductive pattern comprises inner leads 18 having the respective inner tips extending inward to the inside of the device hole 12 and the corresponding outer leads 20 extending outward from the respective inner leads 18 and over the window holes 14. The outer leads 20 are cut at the outer edge of the window holes 14, as shown line P in Fig. 1A, after a semiconductor chip (not shown) is mounted on the TAB tape and hermetically sealed with resin (not shown).

The (wire-bonding type) TAB tape shown in Figs. 1C and 1D is substantially the same as the TAB tape shown in Figs. 1A and 1B, except that the base film 10 has no central device hole, but a conductive die pad 28 is formed at the central position of the TAB tape. Such a conductive die pad 28 can be formed simultaneously with the conductive pattern comprising inner and outer

leads 18 and 20.

The TAB tapes shown in Figs. 1B and 1D are substantially the same as the TAB tapes shown in Figs. 1A and 1C, respectively, except that a tie bar 20a is provided for continuously connecting the outer leads. Such a tie bar 20a can also be formed simultaneously with the conductive pattern comprising inner and outer leads 18 and 20. Also, these tie bars 20a are cut out to separate the adjacent outer leads 20 from each other, as shown lines Q in Figs. 1B and 1D, after a semiconductor chip (not shown) is mounted on the TAB tape and hermetically sealed with resin (not shown).

In Figs. 2A-2D, semiconductor devices using lead frames of Figs. 1A-1D, respectively, are shown. Fig. 3 is a cross-sectional view of the (inner lead bonding type) TAB tape shown semiconductor device of Fig. 2A or 2B. Fig. 4 is a cross-sectional view of the (wire-bonding type) semiconductor device of Fig. 2C or 2D.

In each type of TAB tapes, the thickness of conductive part of the outer lead is increased, in such a manner that the outer lead has a thickness substantially the same as the outer lead of a conventional metal lead frame. Consequently, in the embodiment of this invention, after the copper foil is adhered to the base film 10, the foil is etched to obtain a desired conductive pattern comprising inner leads 18 and the corresponding outer leads 20 and then a nickel is plated, in the same manner as a conventional method. Then, a copper is further plated only on the outer lead portions 20 to increase the thickness thereof. As the thickness of the outer leads 20 are increased, as shown in Figs. 3 and 4, by the copper-plating, the strength can also be increased to substantially the same level as a conventional metal lead frame.

The width of the outer lead 20 can also be increased, as well as the thickness thereof by the above-mentioned copper-plating. However, since the gaps

between the adjacent outer leads 20 are much larger than the gaps between the adjacent inner leads 18, it is effective to plate the outer leads 20 with a copper to increase the thickness of the outer leads 20 to a certain value so as to increase the strength thereof.

In a typical TAB tape, in practice, where the thickness of the inner leads 18 (i.e., the thickness of the copper foil) is about 12-70μm, the thickness of the outer leads 20 can be thus increased to about 125μm.

As clearly shown in Figs. 2A, 2B, 3 and 4, a rectangular or frame-shaped solder resist 22 is coated on the inner leads 18 at a position of the inner leads 18 corresponding to a clamp position of a mold (not shown) which is used, at a later stage, for hermetically sealing the semiconductor device with a resin 26, in such a manner that the gaps between the adjacent inner leads 18 are filled with the resist to prevent the sealing resin 26 from flowing out of the mold (not shown), during a molding process.

In the TAB tapes shown in Figs. 2A, 2B and 3 (i.e., inner lead bonding type TAB tapes), the semiconductor chip 24 is mounted on the TAB tapes, in such a manner that the semiconductor chip 24 is connected to the inner leads 18 by a simultaneous bonding via bumps 18a provided on the surfaces of the semiconductor chip 24. Then, the TAB tape is clamped by the mold (not shown) in the direction of thickness between the base film 10 and solder resist 22 and a resin 26 is then filled in the mold to obtain a hermetically sealed semiconductor device.

On the other hand, in the TAB tape shown in Figs. 2C, 2D and 4, i.e., a wire-bonding type TAB tape, the die pad 28 and the inner leads 18 are mutually supported by the base film portion 30, which maintains the micro-pattern of inner leads 18 to prevent any movement thereof. A semiconductor chip 24 is mounted on the die pad 28 of the TAB tape and, then, the

semiconductor chip 24 is connected to the inner leads 18 by bonding-wires 18b in a conventionally known wire-bonding process. In the same manner as the above, the solder resist 22 is coated against the base film portion 32, in such a manner that the gaps between the adjacent inner leads 18 are filled with the resist to prevent the sealing resin 26 from flowing out of the mold (not shown), during a molding process.

As shown in Figs. 3 and 4, the thickness of the outer leads 20 are increased by the copper-plating, so that the strength of the outer leads 20 is substantially the same as that of a conventional metal lead frame. Therefore, the outer lead portions 20 can easily be handled, and bent, so that the semiconductor device using such a lead frame of the embodiments can easily be mounted on a circuit board (not shown). Also, in the embodiments having a tie-bar 20a as shown in Figs. 2B and 2D, such a tie-bar 20a can easily be removed along the line Q. On the other hand, the inner leads 18 have a thickness much smaller than that of the outer leads 20, so that a TAB tape having fine inner leads, suitable for a high-density semiconductor device, can thus be obtained.

The thickness of the outer leads 20 may be uneven, after the thickness thereof is increased by copper-plating. In that case, the outer leads 20 can be subjected to a coining or pressing process to obtain flat outer leads 20. When the thickness of the outer leads 20 is regulated by the coining or the like, the width thereof can be simultaneously regulated to obtain a desired width.

Figs. 5A-5C are cross-sectional views of some variations of a TAB tape, i.e., a lead frame. An inner lead bonding type TAB tape of Fig. 5A corresponds to the TAB tape shown in Fig. 1A or 1B. A wire-bonding type TAB tape of Fig. 5B corresponds to the TAB tape shown in Fig. 1C or 1D. Another wire-bonding type TAB tape of

Fig. 5C is the same as that of Fig. 5B, except that the TAB tape of Fig. 5C has a device hole 12 and second window holes 14a, so that, as shown in Fig. 7, a semiconductor chip 28 can be mounted on the lower surface of the die-pad 28 and the semiconductor chip 24 can be connected to the inner leads 18 by the bonding wires 18b through the second window holes 14a, which are provided between the central device hole 12 and the first window holes 14.

Figs. 6A-6D are cross-sectional views of some variations of an inner lead bonding-type semiconductor device. In the embodiment of Fig. 6A, the solder resist 22 is coated on the inner leads 18 before the thickness of the outer leads 20 are increased by a copper-plating, so that the thick portion of the outer lead 20 extends from the position of solder resist 22. In the embodiment of Fig. 6B, the solder resist 22 is coated after the thickness of the outer leads 20 are increased by a copper-plating, so that the solder resist 22 is formed on the transitional portion between the thick and thin portions. In the embodiment of Fig. 6C, the solder resist 22 may either be coated before or after the thickness of the outer leads 20 are increased by a copper-plating. In the embodiment of Fig. 6D, no such solder resist (22) is provided and the semiconductor device is hermetically sealed with a resin, in such a manner that the base film 10 may completely covered with the mold resin 26 as shown in the right half of Fig. 6D or the base film 10 may be partially covered as shown in the left half of Fig. 6D.

In the embodiments of Figs. 6B and 6D, the portion of the outer lead 20 where the thickness thereof is increased is covered by the mold resin 26. That is to say, only the thick portion of the outer lead 20 is extended outward from the mold resin 26. Therefore, the outer leads 20, particularly the base portion of the outer leads 20 where the thickness thereof is changed,

can stably be retained by the mold resin 26 and, therefore, the outer leads 20 can be prevented from being easily deformed or bent.

Fig. 7 is a cross-sectional view of a wire-bonding type semiconductor device, in which the semiconductor chip 24 is mounted on the lower surface of the die pad 28 and connected to the inner leads 18 by the bonding wires 18b through the second window holes 14a, as mentioned above with reference to Fig. 5C. Regarding the solder resist 22, although Fig. 7 shows an embodiment in which the solder resist 22 is coated on the inner leads 18 before the thickness of the outer leads 20 is increased by a copper-plating, in the same manner as the embodiment of Fig. 6A. However, such a solder resist 22 can be coated after the copper-plating as the embodiment of Fig. 6B, or such a solder resist 22 may either be coated before or after the copper-plating, as the embodiment of Fig. 6C. Also, there may be no such solder resist (22) as the embodiment of Fig. 6D.

Fig. 8 is a cross-sectional view of another wire-bonding type semiconductor device, in which the semiconductor chip 24 is mounted on the upper surface of the die pad 28 of the TAB tape as shown in Fig. 5B and connected to the inner leads 18 by the bonding wires 18b. Also, in this embodiment, although the solder resist 22 is coated on the inner leads 18 before the copper-plating, in the same manner as the embodiment of Fig. 6A, such a solder resist 22 can be coated after the copper-plating as the embodiment of Fig. 6B, or either before or after the copper-plating as the embodiment of Fig. 6C. Also, there may be no such solder resist (22) as the embodiment of Fig. 6D.

In the embodiment of Fig. 8, if the flexible insulating base film 10, made of such as a polyimide, is replaced by a metal plate, the conductive pattern including the die-pad 28 and inner and outer leads 18 and 22 are formed on the metal plate (10) via an electrically

insulation adhesive layer 10a. In this case, the metal plate (10) can also be used as a heat spreader.

Figs. 9A-9D are cross-sectional views of some variations of a potted type semiconductor device. The embodiments of Figs. 9A-9D are substantially the same as the embodiments of Figs. 6A-6D, respectively, except that a resin 27 is provided to cover the semiconductor chip 24 and the inner leads 18 by potting.

Fig. 10 is a cross-sectional view of an embodiment of a wire-bonding type semiconductor device, which is similar to the embodiment of Fig. 8, except that a resin 27 is provided to cover the semiconductor chip 24 and the inner leads 18 by potting. Also, in this embodiment, although the solder resist 22 is coated on the inner leads 18 before the copper-plating, in the same manner as the embodiment of Fig. 8, such a solder resist 22 can be coated after the copper-plating, or either before or after the copper-plating. Also, there may be no such solder resist (22).

In the same manner as embodiment of Fig. 8, if the base film 10 in the embodiment of Fig. 10 is replaced by a metal plate, the conductive pattern including the die-pad 28 and inner and outer leads 18 and 20 are formed on the metal plate (10) via an electrically insulation adhesive layer 10a. In this case, since the metal plate (10) is directly exposed, a heat from the semiconductor device can be effectively radiated.

In Figs. 11, 12 and 13, some embodiments of a semiconductor device having a heat spreader 34 are shown. The embodiment of Fig. 11 (inner lead-bonding type) is the same as the embodiment of Fig. 6B, except that a heat spreader 34 is disposed for effectively radiating the heat in the semiconductor device. The heat spreader 34 is made of any suitable metal plate having a good thermal conductivity and is shaped such that a central convex portion contacts the semiconductor chip 24, an intermediate bottom portion is exposed to the outside,

and a peripheral portion contacts the base film 10.

The embodiment of Fig. 12 (wire-bonding type) is substantially the same as the embodiment of Fig. 7, except that a heat spreader 34 is disposed in the same manner as the embodiment of Fig. 12. The heat spreader 34 in this embodiment comprises a central convex portion which contacts the die-pad 28 opposite the semiconductor chip 24, an intermediate upper portion exposed to the outside, and a peripheral portion which contacts the solder resist 22.

The embodiment of Fig. 13 (another wire-bonding type) is substantially the same as the embodiment of Fig. 8, except that a heat spreader 34 is disposed in the same manner as the above-mentioned embodiments. The heat spreader 34 in this embodiment comprises a central convex portion which contacts the base film 10 opposite the die-pad 28 and the semiconductor chip 24, an intermediate bottom portion exposed to the outside, and a peripheral portion which also contacts the same base film 10.

In the embodiments of Figs. 8 and 10, instead of an insulating base film made of polyimide, a metal plate made of copper or 42% copper alloy with an electrically insulating layer on the surface thereof is used as a base film. However, such a base film of metal plate can also be used in the embodiments other than those of Figs. 8 and 10.

In the embodiments as mentioned above, the lead frame can be made in accordance with a similar process for making a TAB tape, in which a copper foil is first formed on a base insulating film and then a conductive pattern is formed by etching the copper foil. However, the lead frame can also be made in accordance with a process in which a lead pattern is first formed and then the lead pattern is supported by an insulating film. In any case, the lead frame thus made can be used to mount a semiconductor chip thereon and can be handled in the same manner as a conventional lead frame. A semiconductor

device product sealed with a resin can also be easily handled. Therefore, in this specification, "lead frame" used for mounting thereon a semiconductor chip is also referred to as "TAB tape".

To increase the thickness of a part of the outer lead 20, the outer leads can be plated partially with copper, in the embodiments as mentioned above. However, in practice, the following methods can be employed, in consideration of the bonding characteristic at the inner lead portions and the mounting characteristic at the outer lead portions. In any case, copper can be used as a base material to increase the thickness of the outer leads.

(1) The inner leads are plated with gold to form protective layers and the outer leads are plated with copper or solder to increase the thickness thereof. In this case, since it is relatively difficult to directly plate with gold, it is preferable that the entire lead surfaces including inner and outer leads are plated with nickel as an underlayer, then all of the leads are plated with a gold, and then only the outer lead portions are subjected to plating to increase the thickness thereof.

In this case, to increase the thickness, the outer leads may be plated with copper, plated with solder after plated with copper, or plated with solder in place of copper. Thus, the portions of the outer leads plated with copper or solder, which is exposed to the outside.

(2) Both inner and outer leads are plated with palladium to form protective layers. In this case, in consideration of the bonding characteristic at the inner lead portions and the mounting characteristic at the outer lead portions, all the lead surfaces, including inner and outer leads, are plated with palladium. It is preferable that the copper foil is plated with nickel as an underlayer, then the outer lead portions are subjected to plating to increase the thickness thereof, and then the entire lead surface including inner and outer leads

are plated with palladium. In this case, after the outer lead portions are plated with copper to increase the thickness thereof, solder may further be plated thereon.

(3) Both inner and outer leads are plated with tin to form a protective layer. In this case, since tin can be plated directly on the copper material without an underlayer, only the outer lead portions are first plated with a copper or solder to increase the thickness thereof, and then all the lead surfaces including inner and outer leads are plated with a tin. In this case, the outer lead portions may be first plated with copper and then plated with solder to increase the thickness thereof and then the entire lead surface including inner and outer leads may be plated with tin.

According to this method, since there is no underlayer, the thickness of the inner leads can advantageously be made as thin as possible and, therefore, this method is particularly suitable for making a TAB tape having fine patterns.

In the above-mentioned embodiments, the thickness of the plated layer can advantageously be selected in such a manner that the thickness of the plated gold is 0.3 to 5μm, the thickness of the plated nickel is 1 to 20μm, the thickness of the plated palladium is 0.1 to 0.5μm, and the thickness of the plated tin is about 0.5μm.

The thickness of the plated layer for increasing the thickness of the outer leads may be 50 to 70μm. Since the base copper material has a thickness of about several tens of μm, the entire thickness of the outer lead including the plated underlayer or the like may thus be about 100μm.

Although in the above-mentioned embodiments, the outer leads are subjected to plating to increase the thickness thereof, the thickness of the outer leads 20 may be increased by any other method, such as sputtering, vapor deposition, or the like method.

It should be understood by those skilled in the art

that the foregoing description relates to only a preferred embodiment of the disclosed invention, and that various changes and modifications may be made to the invention without departing from the spirit and scope thereof.

INDUSTRIAL APPLICABILITY

As mentioned above, according to the present invention, a useful and improved lead frame and semiconductor devices using the same can thus be provided.

CLAIMS

1. A lead frame adapted to be used for a semiconductor device comprising:

a plurality of inner leads made of a thin conductive material for easily forming a fine pattern of said inner leads; and

a plurality of outer leads integrally formed with said respective inner leads, said outer leads being coated with metal layers to increase a thickness thereof, so that a desired strength of said outer leads is obtained.

2. A lead frame as set forth in claim 1, wherein said outer leads are plated with a metal which is the same material as said inner and outer leads.

3. A lead frame as set forth in claim 2, wherein all the surfaces of said inner leads and said outer leads are plated with gold, silver, palladium, tin or the like, as a protective metal layer.

4. A lead frame adapted to be used for a semiconductor device comprising:

an insulating base film;

a conductive pattern formed on said insulating base film, said conductive pattern including a plurality of inner leads and a plurality of outer leads integrally formed with said respective inner leads; and

said inner leads being relatively thin, but said outer leads being coated with metal layers to increase the thickness thereof, so that a desired strength of said outer leads is obtained.

5. A lead frame as set forth in claim 4, wherein said outer leads are plated with a metal which is the same material as said inner and outer leads.

6. A lead frame as set forth in claim 5, wherein all the surfaces of said inner leads and said outer leads are plated with gold, silver, palladium, tin or the like, as a protective metal layer.

7. A lead frame as set forth in claim 4, wherein

said insulating base film has a device hole at a central position thereof and window holes located apart from said central device hole, each said inner lead extends inward into said central device hole and each said outer lead extends outward from said inner lead over said window hole.

8. A lead frame as set forth in claim 4, wherein a die-pad is formed as a part of said conductive pattern formed on said insulating base film at a central position thereof, and said insulating base film has window holes located apart from said die-pad, each said inner lead extends toward said die-pad and each said outer lead extends outward from said inner lead over said window hole.

9. A lead frame as set forth in claim 4, wherein said outer leads are continuously connected to each other by means of a tie bar which is a part of said conductive pattern formed on said insulating base film.

10. A process for making a lead frame adapted to be used for a semiconductor device which comprises the steps of:

forming a conductive layer on a insulating base film;

etching said conductive layer to form a conductive pattern including a plurality of inner leads and a plurality of outer leads integrally formed with said respective inner leads; and

coating said outer leads with metal layers to increase the thickness of said outer leads, so that a desired strength of said outer leads is obtained.

11. A process as set forth in claim 10, wherein said coating step comprises a step of plating said outer leads with a metal which is the same material as said inner and outer leads to increase the thickness of said outer leads.

12. A process as set forth in claim 11, wherein said coating step comprises a step of plating all the

surfaces at said inner leads and said outer leads with gold, silver, palladium, tin or the like, as a protective metal layer.

13. A process for making a lead frame adapted to be used for a semiconductor device which comprises the steps of:

forming a conductive layer on an insulating base film having a device hole at a central position thereof and window holes located apart from said central device hole;

etching said conductive layer to form a conductive pattern including a plurality of inner leads and a plurality of outer leads integrally formed with said respective inner leads, so that each said inner lead extends inward into said central device hole and each said outer lead extends outward from said inner lead over said window hole; and

coating said outer leads with metal layers to increase the thickness thereof, so that a desired strength of said outer leads is obtained.

14. A process for making a lead frame adapted to be used for a semiconductor device which comprises the steps of:

forming a conductive layer on an insulating base film having window holes located apart from a central position of said base film;

etching said conductive layer to form a conductive pattern including a die-pad located at a central position of said insulating base film, a plurality of inner leads and a plurality of outer leads integrally formed with said respective inner leads, so that each said inner lead extends toward said die-pad and each said outer lead extends outward from said inner lead over said window hole; and

coating said outer leads with metal layers to increase the thickness thereof, so that a desired strength of said outer leads is obtained.

15. A semiconductor device comprising:

(a) a lead frame adapted to be used for a semiconductor device comprising:

a plurality of inner leads made of a thin conductive material for easily forming a fine pattern of said inner leads; and

a plurality of outer leads integrally formed with said respective inner leads, said outer leads being coated with metal layers to increase the thickness thereof, so that a desired strength of said outer leads is obtained;

(b) a semiconductor chip electrically connected to said inner leads; and

(c) a resin for hermetically sealing said semiconductor chip and a part of said lead frame including said inner leads.

16. A semiconductor device comprising:

(a) a lead frame comprising:

an insulating base film having a device hole at a central position thereof and window holes located apart from said device hole;

a conductive pattern formed on said insulating base film, said conductive pattern including a plurality of inner leads and a plurality of outer leads integrally formed with said respective inner leads, so that each said inner lead extends inward into said central device hole and each said outer lead extends outward from said inner lead over said window hole; and

said inner leads being relatively thin, but said outer leads being coated with metal layers to increase the thickness thereof, so that a desired strength of said outer leads is obtained;

(b) a semiconductor chip mounted on and electrically connected to said inner leads within said central opening; and

(c) a resin for hermetically sealing said semiconductor chip and a part of said lead frame

including said inner leads.

17. A semiconductor device comprising:

(a) a lead frame comprising:

an insulating base film having window holes located apart from a central position of said base film;

a conductive pattern formed on said insulating base film, said conductive pattern including a plurality of inner leads and a plurality of outer leads integrally formed with said respective inner leads, so that each said inner lead extends toward said die-pad and each said outer lead extends outward from said inner lead over said window hole; and

said inner leads being relatively thin, but said outer leads being coated with metal layers to increase the thickness thereof, so that a desired strength of said outer leads is obtained;

(b) a semiconductor chip mounted on said die-pad;

(c) bonding wires for electrically connecting said semiconductor chip to said inner leads; and

(d) a resin for hermetically sealing said semiconductor chip and a part of said lead frame including said inner leads.

Fig.1A

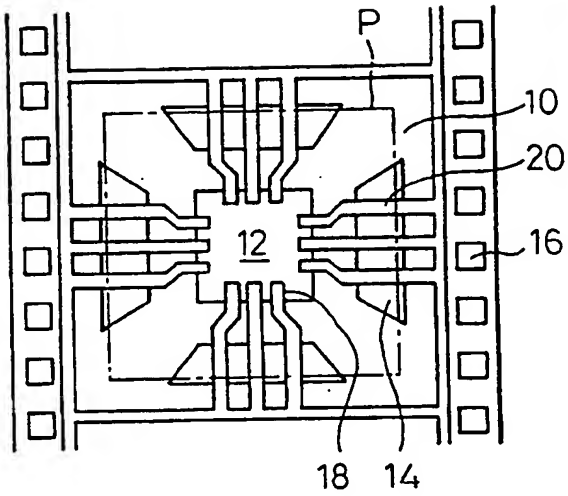


Fig.1C

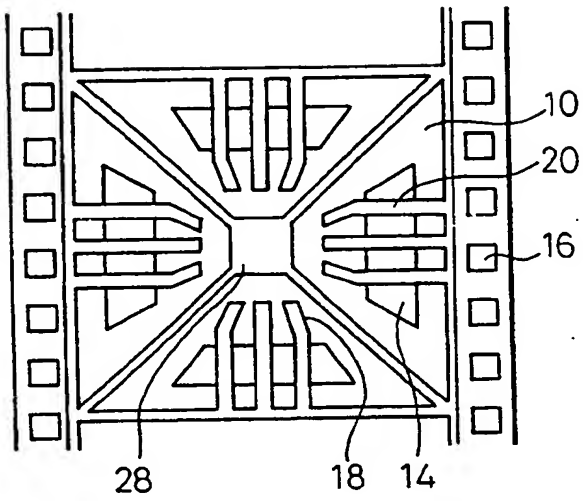


Fig.1B

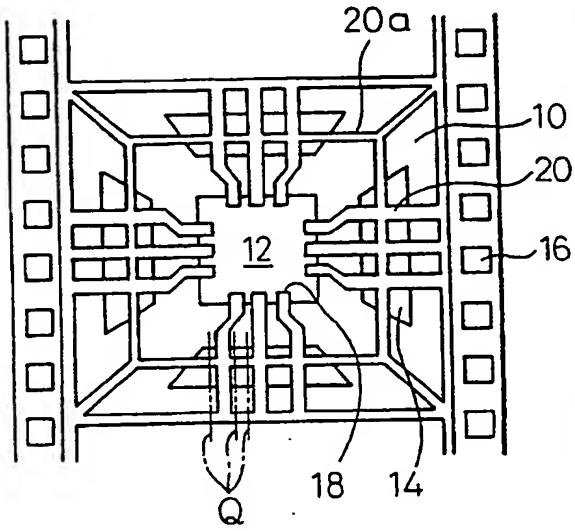


Fig.1D

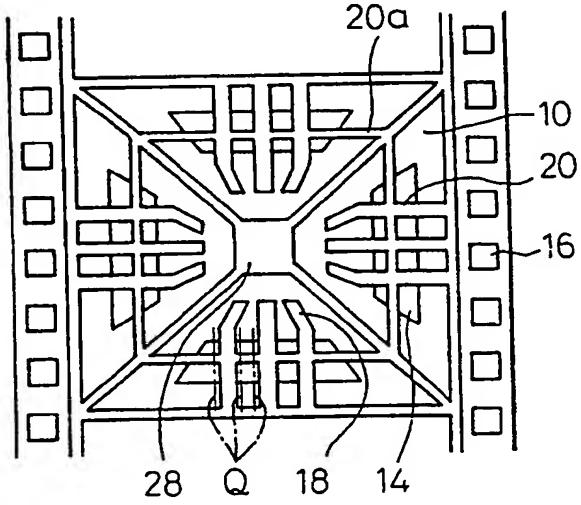


Fig.2A

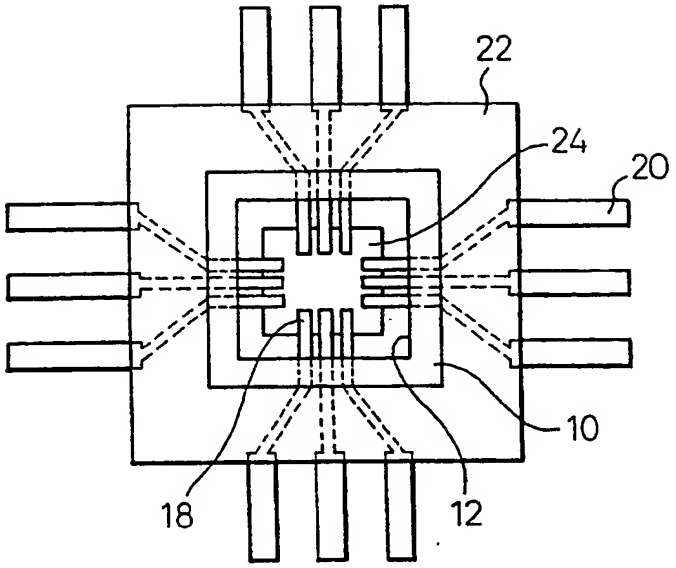


Fig.2B

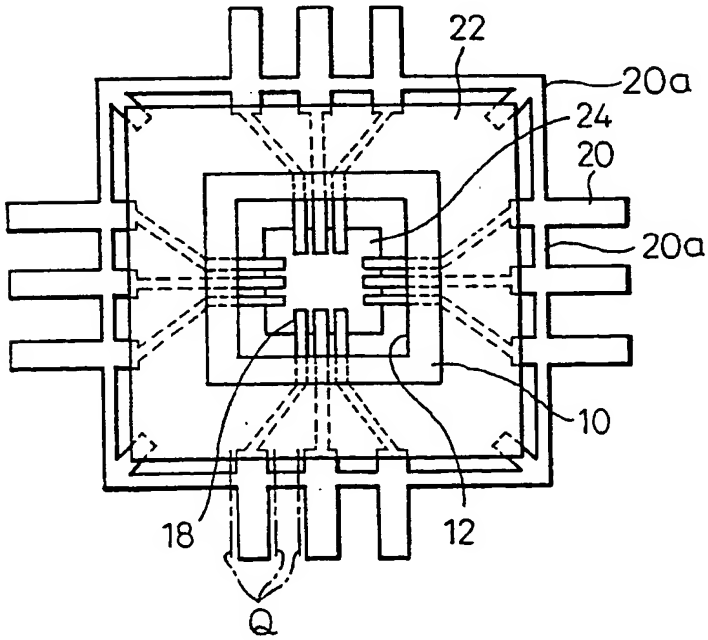


Fig.2C

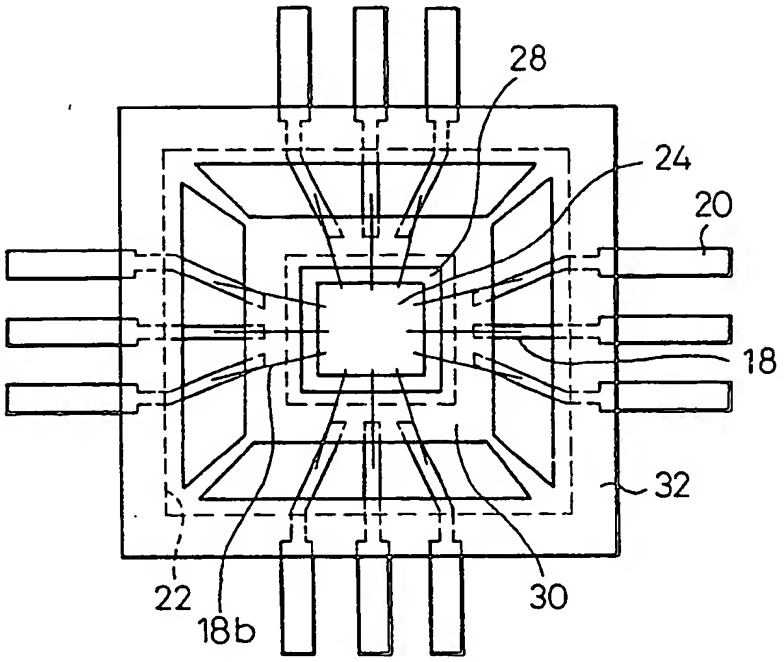


Fig.2D

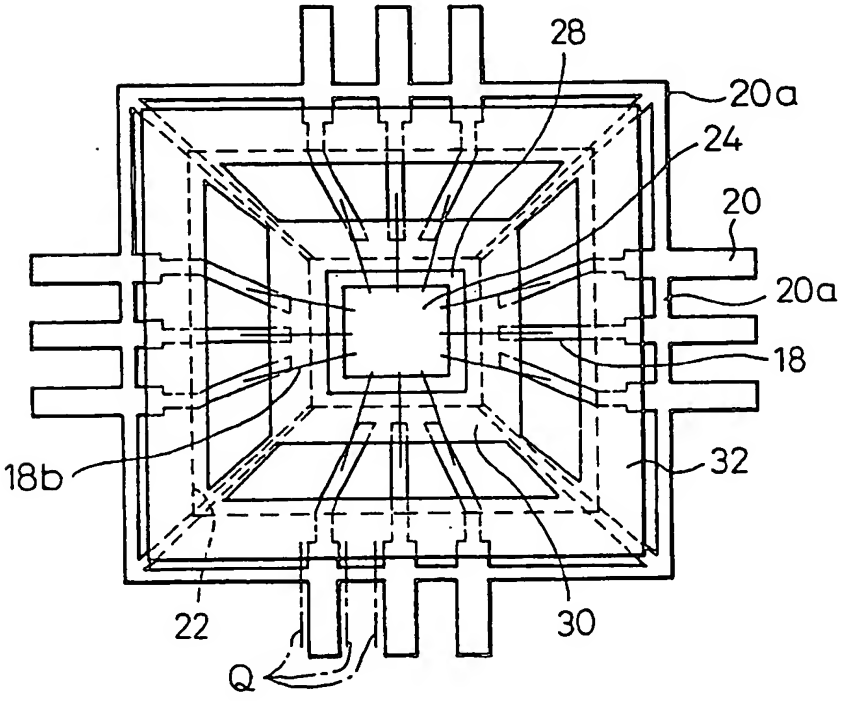


Fig.3

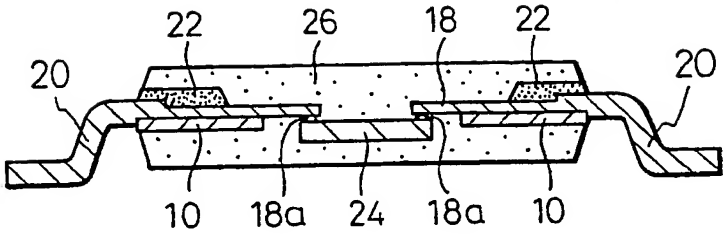


Fig.4

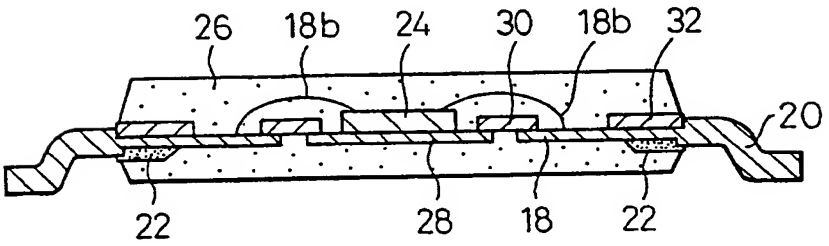


Fig.5A

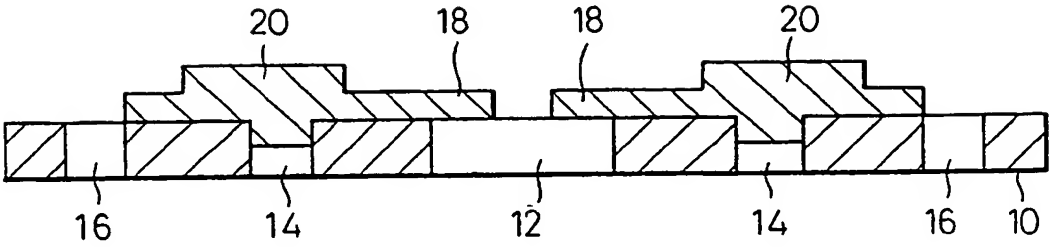


Fig.5B

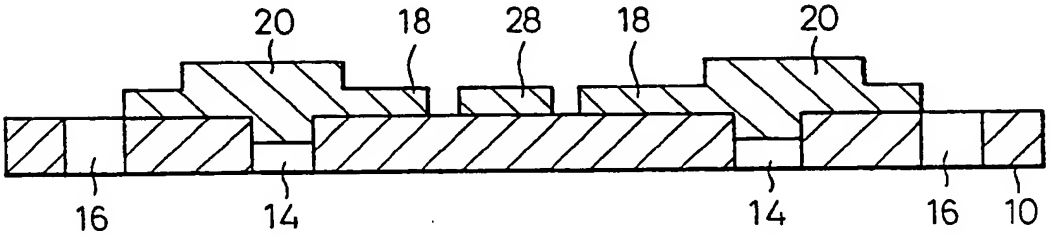


Fig.5C

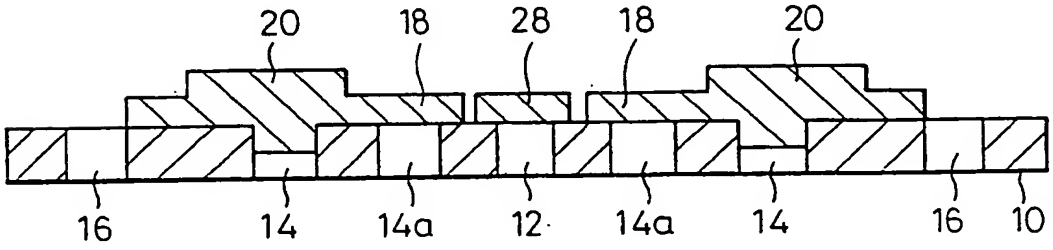


Fig.6A

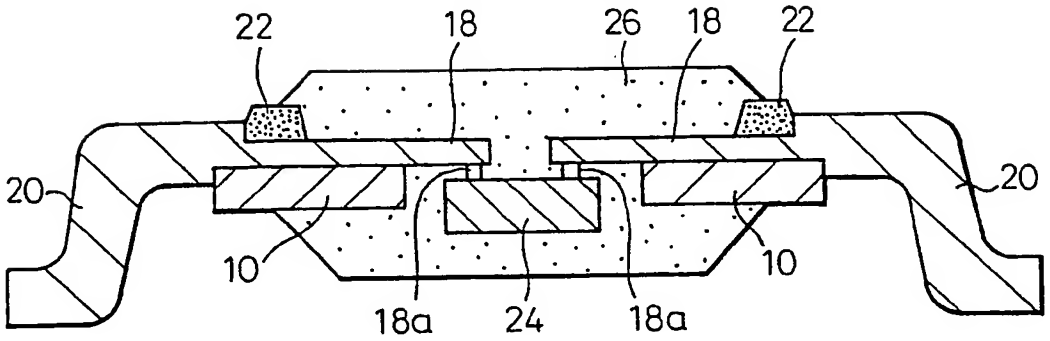


Fig.6B

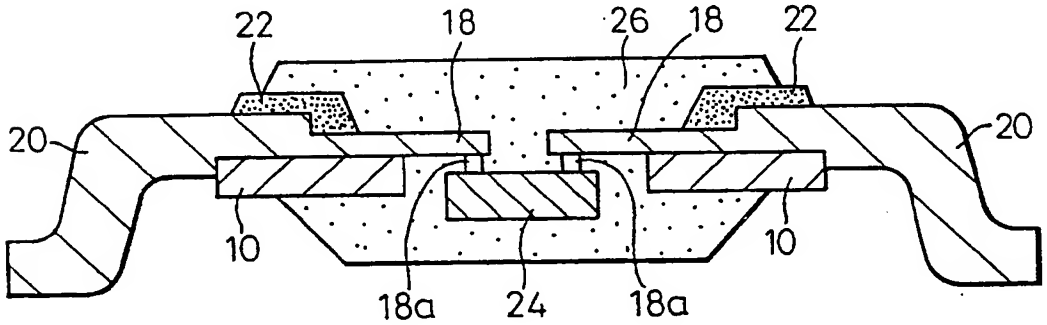


Fig.6C

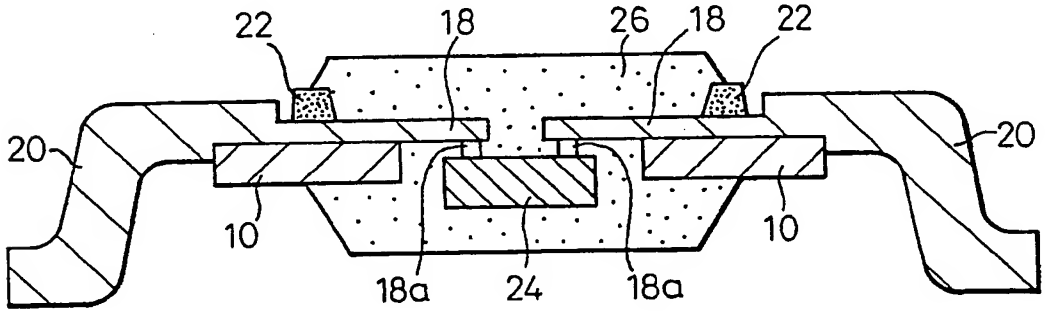


Fig.6D

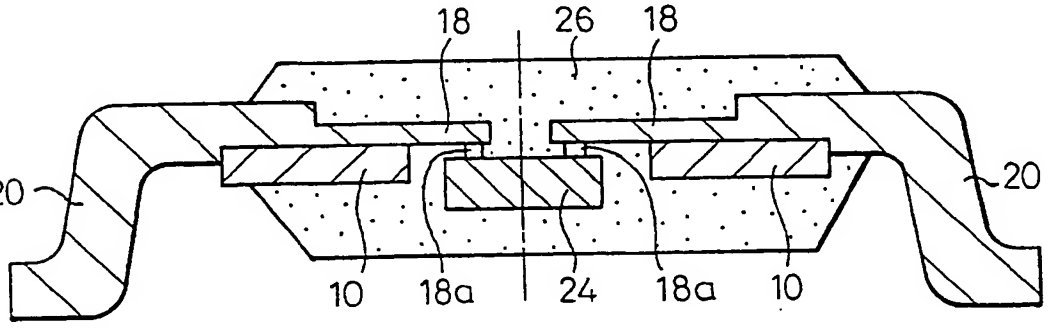


Fig.7

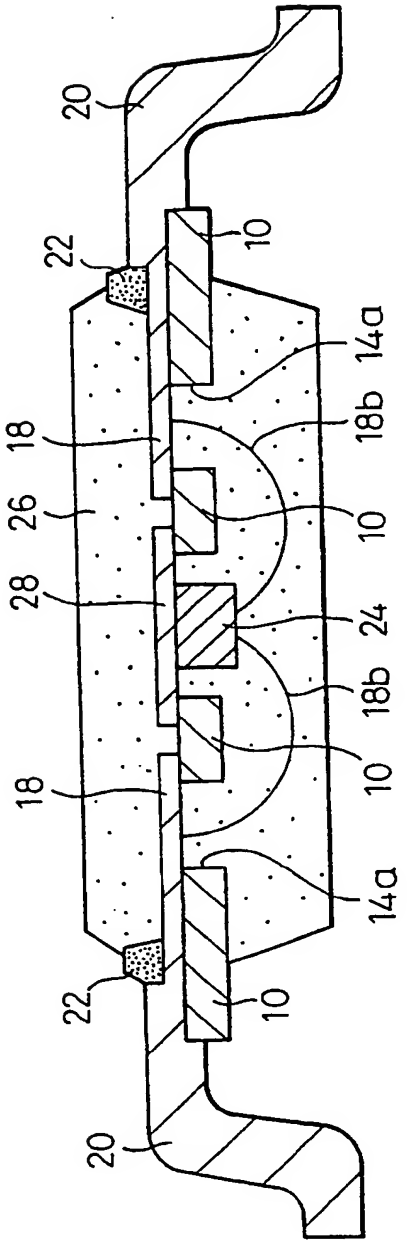


Fig.8

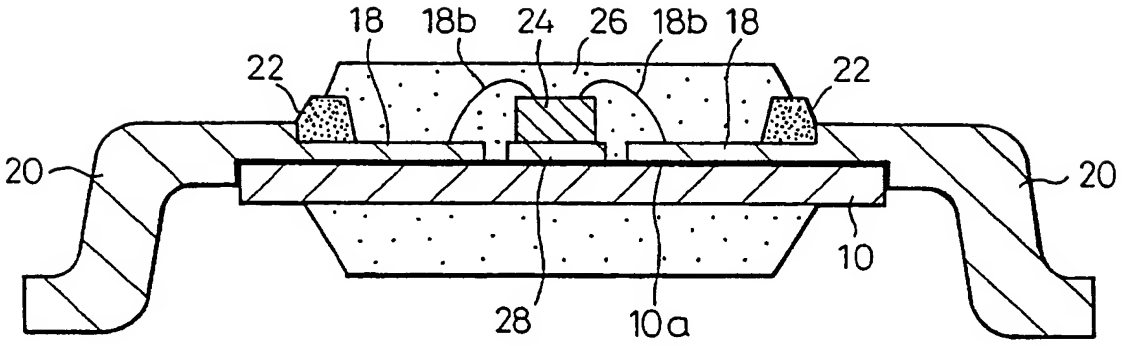


Fig.9A

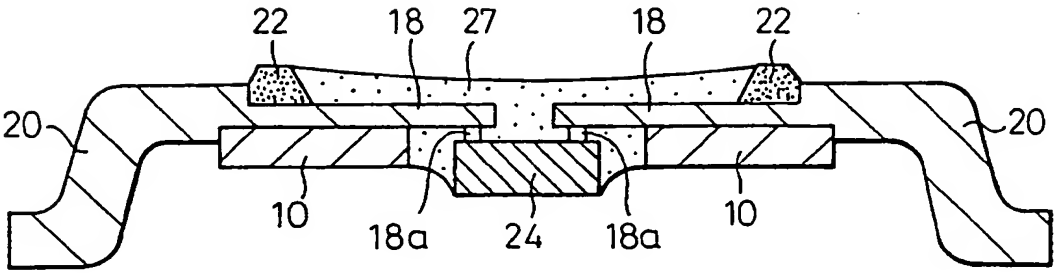


Fig.9B

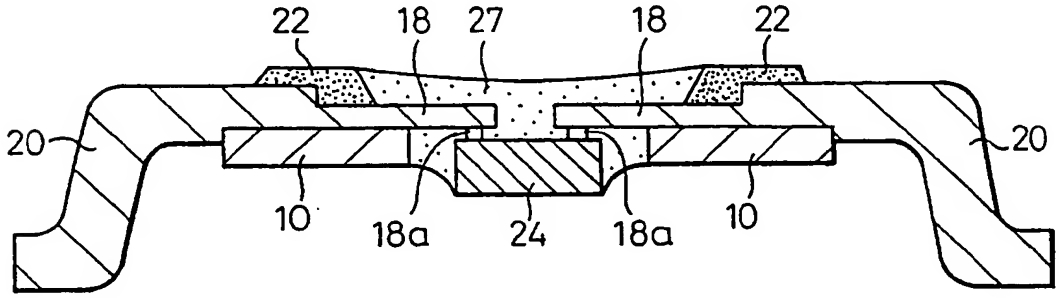


Fig.9C

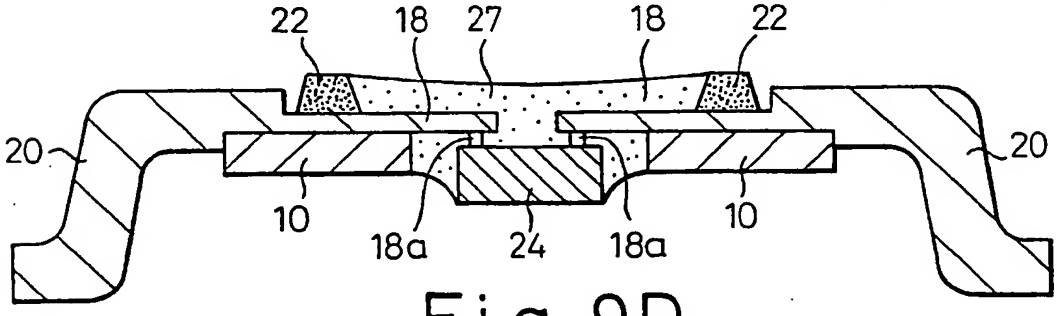


Fig.9D

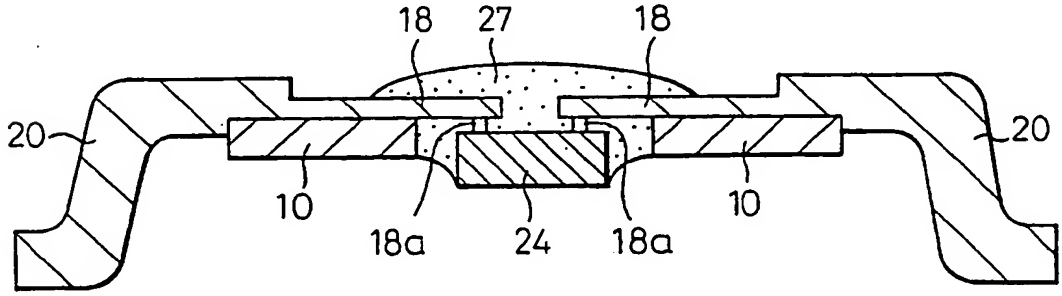
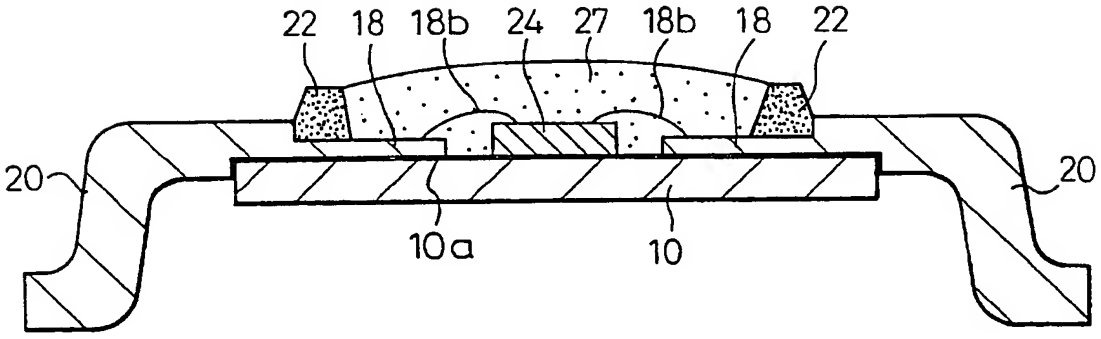


Fig.10


22
18
18b
24
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18b
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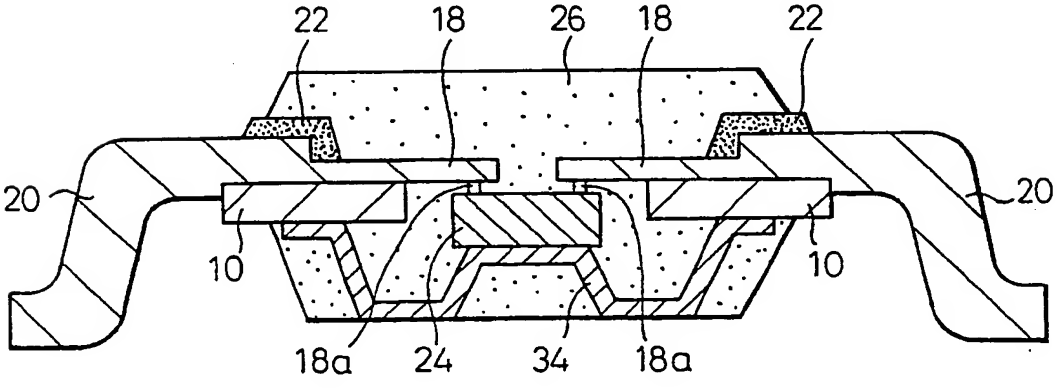
Fig.11


22
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18
22
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20
10
10
18a
24
34
18a

Fig.12

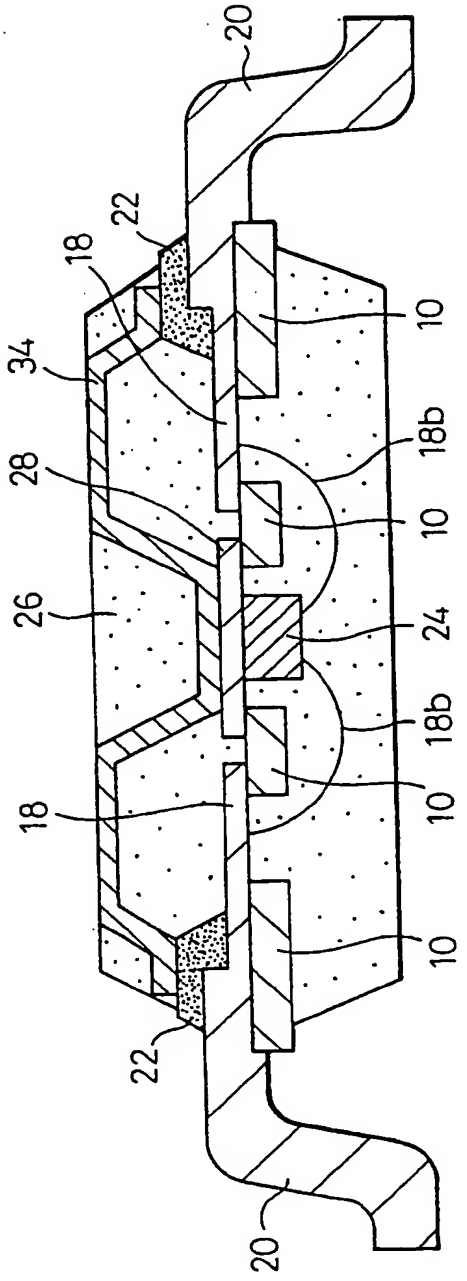
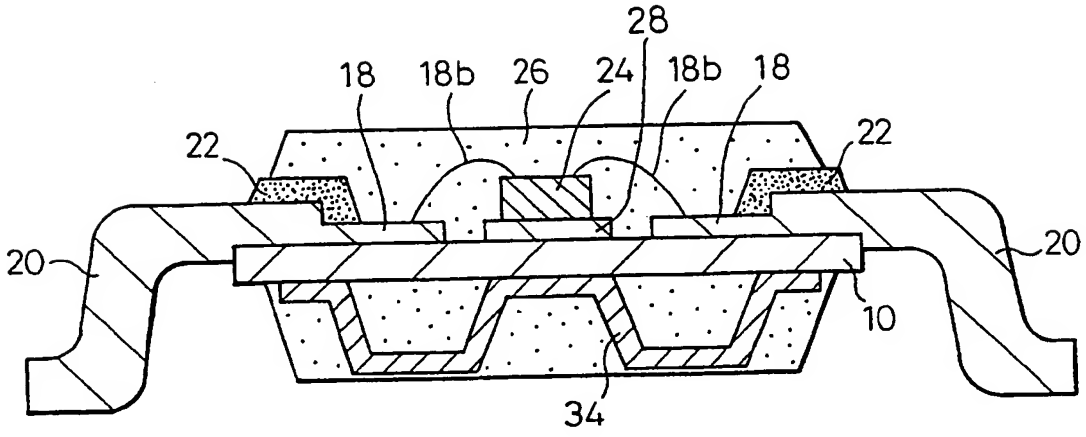


Fig.13



INTERNATIONAL SEARCH REPORT

Internat · Application No
PCT/JP 93/01677

A. CLASSIFICATION OF SUBJECT MATTER
IPC 5 H01L23/495 H01L21/48

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 5 H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X A	US,A,4 707 724 (SUZUKI ET AL) 17 November 1987 see column 3, line 66 - column 4, line 15; figure 1	1,15 4,16,17
X	PATENT ABSTRACTS OF JAPAN vol. 14, no. 576 (E-1016)21 December 1990 & JP,A,02 250 364 (TOPPAN PRINTING CO LTD) see abstract	1
X	PATENT ABSTRACTS OF JAPAN vol. 13, no. 044 (E-710)31 January 1989 & JP,A,63 239 829 (HITACHI LTD) see abstract	4

-/--

[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

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"O" document referring to an oral disclosure, use, exhibition or other means

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"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
4 February 1994	22.02.94
Name and mailing address of the ISA European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax (+31-70) 340-3016	Authorized officer Greene, S

Form PCT/ISA/210 (second sheet) (July 1992)

INTERNATIONAL SEARCH REPORT

Internat ' Application No
PCT/JP 93/01677

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
		4
X	PATENT ABSTRACTS OF JAPAN vol. 12, no. 49 (E-582)13 February 1988 & JP,A,62 196 840 (OKI ELECTRIC IND CO LTD) see abstract	
A	AT,B,315 947 (INTERELECTRIC AG) see page 2, line 28 - line 52	1,4,10, 12-14
		4
A	PATENT ABSTRACTS OF JAPAN vol. 16, no. 340 (E-1238)3 April 1992 & JP,A,04 102 341 (SHINKO ELECTRIC CO LTD$) see abstract	

1

INTERNATIONAL SEARCH REPORT

Information on patent family members

Internati · · Application No
PCT/JP 93/01677

Patent document cited in search report	Publication date	Patent family member(s)		Publication date
US-A-4707724	17-11-87	JP-A-	60257160	18-12-85
		KR-B-	9310073	14-10-93
AT-B-315947	15-05-74	AT-A,B	315947	15-05-74